AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1. (Currently Amended) A method for generating a fixed angle delayed clock signal as compared to a reference clock signal while compensating for skew introduced by system clock delay, the method comprising the following:

an act of passing a reference clock signal through a reference clock delay line comprising a plurality of reference clock delay elements;

an act of adjusting a number of reference clock delay elements through which the reference clock signal passes in the reference clock delay line until the reference clock signal at [[the]] an output terminal of the reference clock delay line and received at a feedback clock input of a phase detector and the reference clock signal received at a reference input terminal of the phase detector are approximately in phase;

an act of calculating an initial number of fixed angle clock delay elements in a fixed angle clock delay line needed to generate a fixed angle delayed clock signal with respect to the reference clock signal, the calculation being based on the number of reference clock delay elements used at the time the reference clock signal at the reference input of the phase detector and the reference clock signal at the feedback clock input of the phase detector are approximately in phase;

an act of receiving a clock signal from the fixed angle clock delay line;

an act of passing the clock signal through a system clock mechanism that introduces the system clock delay;

an act of calculating an adjustment number of fixed angle clock delay elements needed to account for the system clock delay using the clock signal received from the fixed angle clock delay line and the clock signal after having passed through the system clock mechanism;

an act of calculating a final number of fixed angle clock delay elements needed to generate a fixed angle delayed clock signal that accounts for the system clock delay by adjusting the initial number of fixed angle clock delay elements by the adjustment number of fixed angle clock delay elements;

an act of receiving the reference clock signal at an input terminal of the fixed angle clock delay line; and

an act of passing the reference clock signal through the final number of fixed angle clock delay elements before allowing the reference clock signal to be output from the fixed angle clock delay line in the form of the fixed angle delayed clock signal that accounts for system clock delay.

Claim 2. (Original) A method in accordance with Claim 1, wherein the fixed angle delay clock signal is approximately ninety degrees ahead of the reference clock signal after accounting for system clock delay.

Claim 3. (Original) A method in accordance with Claim 1, wherein the fixed angle delay clock signal is approximately one hundred and eighty degrees ahead of the reference clock signal after accounting for system clock delay.

Claim 4. (Original) A method in accordance with Claim 1, wherein the fixed angle delay clock signal is approximately two hundred and seventy degrees ahead of the reference clock signal after accounting for system clock delay.

Claim 5. (Original) A method in accordance with Claim 1, wherein the fixed angle delayed clock signal is a first quadrature clock signal, the fixed angle clock delay line is a first quadrature clock delay line, the fixed angle clock delay elements are first quadrature clock delay elements, the clock signal is a first clock signal, the system clock mechanism is a first system clock mechanism, and the system clock delay is first system clock delay, the method further generating a second quadrature clock signal of a different quadrature than the first quadrature clock signal while still accounting for a second system clock delay, the method further comprising the following:

an act of calculating an initial number of second quadrature clock delay elements in a second quadrature clock delay line needed to generate a second quadrature clock signal of the reference clock signal, the calculation being based on the number of reference clock delay elements used at the time the reference clock signal at the reference input of the phase detector and the reference clock signal at the feedback clock input of the phase detector are approximately in phase;

an act of receiving a second clock signal from the second quadrature clock delay line;

an act of passing the second clock signal through a second system clock mechanism that introduces the second system clock delay;

an act of calculating an adjustment number of second quadrature clock delay elements needed to account for the second system clock delay using the second clock signal received from the second quadrature clock delay line and the second clock signal after having passed through the second system clock mechanism;

an act of calculating a final number of second quadrature clock delay elements needed to generate a second quadrature clock signal that accounts for the second system clock delay by adjusting the initial number of second quadrature clock delay elements by the adjustment number of second quadrature clock delay elements;

an act of receiving the reference clock signal at an input terminal of the second quadrature clock delay line; and

an act of passing the reference clock signal through the final number of second quadrature clock delay elements before allowing the reference clock signal to be output from the second quadrature clock delay line in the form of the second quadrature clock signal that accounts for the second system clock delay.

Claim 6. (Original) A method in accordance with Claim 5, wherein the first quadrature clock signal is approximately ninety degrees ahead of the reference clock signal after accounting for the first system clock delay, and the second quadrature clock signal is approximate one hundred and eighty degrees ahead of the reference clock signal after accounting for the second system clock delay.

Claim 7. (Original) A method in accordance with Claim 5, wherein the first quadrature clock signal is approximately ninety degrees ahead of the reference clock signal after

accounting for the first system clock delay, and the second quadrature clock signal is approximate two hundred and seventy degrees ahead of the reference clock signal after accounting for the second system clock delay.

Claim 8. (Original) A method in accordance with Claim 5, wherein the first quadrature clock signal is approximately one hundred and eighty degrees ahead of the reference clock signal after accounting for the first system clock delay, and the second quadrature clock signal is approximate two hundred and seventy degrees ahead of the reference clock signal after accounting for the second system clock delay.

Claim 9. (Original) A method in accordance with Claim 5, the method further generating a third quadrature clock signal of a different quadrature than the first and second quadrature clock signals while still accounting for a third system clock delay, the method further comprising the following:

an act of calculating an initial number of third quadrature clock delay elements in a third quadrature clock delay line needed to generate a third quadrature clock signal of the reference clock signal, the calculation being based on the number of reference clock delay elements used at the time the reference clock signal at the reference input of the phase detector and the reference clock signal at the feedback clock input of the phase detector are approximately in phase;

an act of receiving a third clock signal from the third quadrature clock delay line;

an act of passing the third clock signal through a third system clock mechanism that introduces the third system clock delay;

an act of calculating an adjustment number of third quadrature clock delay elements needed to account for the third system clock delay using the third clock signal received from the third quadrature clock delay line and the third clock signal after having passed through the third system clock mechanism;

an act of calculating a final number of third quadrature clock delay elements needed to generate a third quadrature clock signal that accounts for the third system clock delay by adjusting the initial number of third quadrature clock delay elements by the adjustment number of third quadrature clock delay elements;

an act of receiving the reference clock signal at an input terminal of the third quadrature clock delay line; and

an act of passing the reference clock signal through the final number of third quadrature clock delay elements before allowing the reference clock signal to be output from the third quadrature clock delay line in the form of the third quadrature clock signal that accounts for the third system clock delay.

Claim 10. (Original) A method in accordance with Claim 9, wherein the first quadrature clock signal is approximately ninety degrees ahead of the reference clock signal after accounting for the first system clock delay, the second quadrature clock signal is approximate one hundred and eighty degrees ahead of the reference clock signal after accounting for the second system clock delay, and the third quadrature clock signal is approximately two hundred and seventy degrees ahead of the reference clock signal after accounting for the third system clock delay.

Claim 11. (Original) A method in accordance with Claim 1, further comprising the following:

an act of periodically repeating an act of sampling, wherein the act of sampling comprises the following:

the act of calculating an initial number of fixed angle clock delay elements in a fixed angle clock delay line needed to generate a fixed angle delayed clock signal with respect to the reference clock signal, the calculation being based on the number of reference clock delay elements used at the time the reference clock signal at the reference input of the phase detector and the reference clock signal at the feedback clock input of the phase detector are approximately in phase;

the act of receiving a clock signal from the fixed angle clock delay line;

the act of passing the clock signal through a system clock mechanism that introduces the system clock delay;

the act of calculating an adjustment number of fixed angle clock delay elements needed to account for the system clock delay using the clock signal received from the fixed angle clock delay line and the clock signal after having passed through the system clock mechanism;

the act of calculating a final number of fixed angle clock delay elements needed to generate a fixed angle delayed clock signal that accounts for the system clock delay by adjusting the initial number of fixed angle clock delay elements by the adjustment number of fixed angle clock delay elements;

the act of receiving the reference clock signal at an input terminal of the fixed angle clock delay line; and

the act of passing the reference clock signal through the final number of fixed angle clock delay elements before allowing the reference clock signal to be output from the fixed angle clock delay line in the form of the fixed angle delayed clock signal that accounts for system clock delay.

Claim 12. (Original) A method in accordance with Claim 11, further comprising the following:

an act of determining that the digital delay locked loop is in pseudo lock,

wherein the act of sampling is repeated more frequently prior to the act of determining than after the act of determining.

Claim 13. (Original) A method in accordance with Claim 1, wherein the phase detector is configured to generate a first signal when the phase of the reference clock signal at the reference input of the phase detector is not approximately equal to the phase of the reference clock signal at the feedback clock input of the phase detector and the variance is in a first direction, wherein the phase detector is further configured to generate a second signal when the phase of the reference clock signal at the reference input of the phase detector is not approximately equal to the phase of the reference clock signal at the feedback clock input of the phase detector and the variance is in a second direction that is opposite the first direction, a method for adjusting the number of reference clock delay elements through which the reference clock signal passes in the reference clock delay line, the method comprising the following:

an act of a filter receiving a first signal from the phase detector;

an act of the filter determining whether the reception of the first signal results in a predetermined number of consecutive first signals being received from the phase detector;

an act of filter adjusting the adjustable number of reference clock delay elements through which the reference clock signal passes in the reference clock delay line if there has been the predetermined number of consecutive first signals received from the phase detector, and otherwise not adjusting the number of reference clock delay elements.

Claim 14. (Currently Amended) A method in accordance with Claim 1, further comprising the following:

an act of determining whether the clock signal at [[the]] <u>an</u> output terminal of the fixed angle clock delay line and after passing through the system clock mechanism is approximately in phase with the clock signal before passing through the fixed angle clock delay line, or whether there is a variance.

Claim 15. (Original) A method in accordance with Claim 14, further comprising the following:

an act of changing a value of a variable in a first direction if there is a variance in a first direction, and otherwise changing a value of the variable in a second direction opposite the first direction;

an act of identifying whether the act of changing a value of a variable results in the value meeting or exceeding a predetermined threshold value; and

an act of changing a status of a lock determination from locked to unlocked or vice versa, if the value has been changed to meet or exceed the predetermined threshold value, and otherwise keeping a lock status the same.

Claim 16. (Original) A method in accordance with Claim 1, wherein the method is implemented by a delay locked loop circuit that includes the reference clock delay line, the phase detector, and a control circuit configured to adjust the number of reference clock delay elements through which the reference clock signal passes in response to a signal from the phase detector circuit, the method further comprising the following:

an act the control circuit receiving a disable signal indicating that the adjustable number of reference clock delay element is not to be adjusted for at least a period of time;

an act of the control circuit receiving one or more signal from the phase detector that would cause the control circuit to adjust the number of reference clock delay elements through which the reference clock signal passes had the disable signal not been received; and

an act of the control circuit maintaining the number of reference delay elements through which the reference clock signal passes to be the same during the period of time despite the control circuit having received the one or more signals from the phase detector.

Claim 17. (Original) A delay locked loop circuit configured to generate a fixed angle delayed clock signal as compared to a reference clock signal while compensating for system clock delay, the delay locked loop circuit comprising the following:

a reference clock delay line configured to receive the reference clock signal and pass the reference clock signal through an adjustable number of reference clock delay elements;

a reference clock phase detector circuit having a reference input coupled to receive at least a derivative of the reference clock signal at a reference input, and coupled to receive the reference clock signal after having passed through the reference clock delay line at a feedback clock input, the reference clock phase detector configured to detect whether the reference clock signal at the reference input of the phase detector and the reference clock signal at the feedback clock input of the phase detector are approximately in phase;

a reference clock control circuit configured to adjust the number of reference clock delay elements through which the reference clock signal passes in response to the detection of the reference clock phase detector;

a fixed angle clock delay line configured to receive an input clock signal that is at least derived from the reference clock signal, and pass the input clock signal through an adjustable number of fixed angle clock delay elements;

a system clock adjustment circuit configured to calculate an adjustment number of fixed angle clock delay elements needed to account for the system clock delay;

a fixed angle clock control circuit configured to perform the following:

an act of calculating an initial number of fixed angle clock delay elements in the fixed angle clock delay line needed to generate a fixed angle delayed clock signal of the reference clock signal, the calculation being based on the number of reference clock delay elements used at the time the reference clock signal at the reference input of the reference clock phase detector and the reference clock signal at the feedback clock input of the reference clock phase detector are approximately in phase;

an act of calculating a final number of quadrature clock delay elements needed to generate a fixed angle delayed clock signal that accounts for system clock delay by

adjusting the initial number of fixed angle clock delay elements by the adjustment number of fixed angle clock delay elements; and

an act of adjusting the number of fixed angle clock delay elements through which the input clock signal passes in the fixed angle clock delay line to be equal to the calculated final number of fixed angle clock delay elements.

Claims 18 and 19. (Cancelled).

Claim 20. (Currently Amended) In a delay locked loop circuit that includes a delay line configured to receive a clock signal and pass the clock signal through an adjustable number of delay elements, a phase detector circuit configured to sample a phase of a clock signal at an output terminal of the delay line and received at a feedback clock input of the phase detector and the clock signal received at a reference input of the phase detector, the phase detector configured to generate a first signal when the phase of the clock signal at the feedback clock input of the phase detector is not approximately equal to the phase of the reference clock signal at a reference input of the phase detector and the variance is in a first direction, wherein the phase detector is further configured to generate a second signal when the phase of the clock signal at the feedback clock input of the phase detector is not approximately equal to the phase of the reference clock signal at the reference input of the phase detector and the variance is in a second direction that is opposite the first direction, a method for adjusting the number of delay elements through which the clock signal passes in the delay line, the method comprising the following:

an act of a filter receiving a first signal from the phase detector;

an act of determining whether the reception of the first signal results in a predetermined number of <u>multiple</u> consecutive first signals being received from the phase detector;

an act of adjusting the adjustable number of delay elements through which the clock signal passes in the delay line if there has been the predetermined number of <u>multiple</u> consecutive first signals received from the phase detector, and otherwise not adjusting the number of delay elements.

Claim 21. (Currently Amended) A method in accordance with Claim 20, wherein the predetermined <u>multiple</u> number is a first predetermined number, the method further comprising the following:

an act of the filter receiving a second signal from the phase detector;

an act of determining whether the reception of the second signal results in a second predetermined <u>multiple</u> number of consecutive second signals being received from the phase detector;

an act of adjusting the adjustable number of delay elements through which the clock signal passes in the delay line if there has been the second predetermined <u>multiple</u> number of consecutive second signals received from the phase detector, and otherwise not adjusting the number of delay elements.

Claim 22. (Currently Amended) A method in accordance with Claim 21, wherein the first predetermined <u>multiple</u> number is the same as the second predetermined number.

Claim 23. (Currently Amended) A method in accordance with Claim 21, wherein the act of adjusting the adjustable number of delay elements through which the clock signal passes in the delay line if there has been the first predetermined multiple number is performed in a different direction as when performing the act of adjusting the adjustable number of delay elements through which the clock signal passes in the delay line if there has been the second predetermined multiple number.

Claim 24. (Cancelled).

Claim 25. (Currently Amended) A method in accordance with Claim 24, wherein the predetermined multiple number is more than two.

Claim 26. (Currently Amended) A method in accordance with Claim 25, wherein the predetermined multiple number is eight.

Claim 27. (Currently Amended) A method in accordance with Claim 20, wherein the act determining whether the reception of the first signal results in a predetermined multiple number of consecutive first signals being received from the phase detector further comprises the following:

an act of determining whether the reception of the first signal results in a predetermined multiple number of consecutive first signals being received from the phase detector, the predetermined multiple number of consecutive first signals being uninterrupted in time from a flush signal in which the filter memory is reset.

Claim 28. (Currently Amended) A delay locked loop circuit comprising the following:

a delay line configured to receive a clock signal and pass the clock signal through an adjustable number of delay elements;

a phase detector configured to compare a phase of a clock signal at an output terminal of the delay line and received at a feedback clock input of the phase detector and the clock signal received at a reference input of the phase detector, and configured to generate a first signal when the phase of the clock signal at the feedback clock input of the phase detector is not approximately equal to the phase of the reference clock signal at a reference input of the phase detector and the variance is in a first direction, wherein the [[control]] phase detector is further configured to generate a second signal when the phase of the feedback clock input of the phase detector is not approximately equal to the phase of the reference clock signal at a reference input of the phase detector and the variance is in a second direction that is opposite the first direction;

a filter configured to perform the following:

an act of receiving a first signal from the phase detector;

an act of determining whether the reception of the first signal results in a predetermined multiple number of consecutive first signals received from the phase detector;

an act of causing an adjustment in the adjustable number of delay elements through which the clock signal passes in the delay line if there has been the predetermined multiple number of consecutive first signals received from the phase detector ~~control circuit~~, and otherwise not adjusting the number of delay elements.

Claims 29 and 30. (Cancelled).